ADS8568EVM-PDK

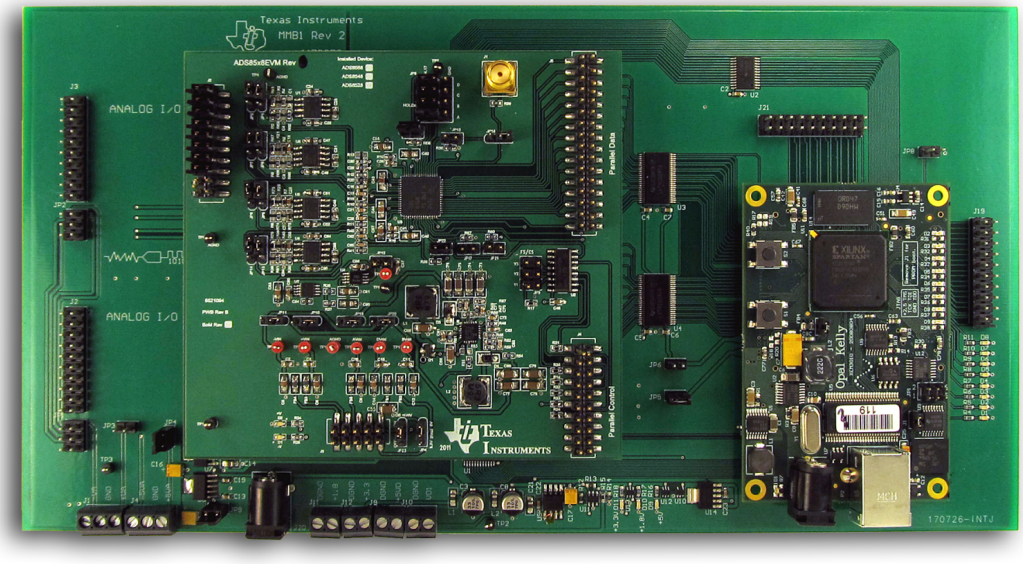

Figure 1. ADS8568EVM-PDK

This user's guide describes the characteristics, operation, and use of the ADS8568EVM by itself and as part of the ADS8568EVM-PDK. This evaluation module (EVM) is an evaluation platform for the ADS8568, a 16-bit, eight-channel, simultaneous sampling, bipolar input analog-to-digital converter (ADC). The ADS8568EVM allows evaluation of all aspects of the ADS8568 device. This document includes an EVM QuickStart, hardware and software details, bill of materials, and schematic.

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1 EVM Overview

The ADS8568EVM is an evaluation module (EVM) built to the TI Modular EVM System specification. It can be connected to any of the modular EVM system interface cards available from Texas Instruments. The ADS8568EVM is available as a stand-alone printed circuit board (PCB) or as part of the ADS8568EVM-PDK, which includes an MMB1 motherboard and software. As a stand-alone PCB, the ADS8568EVM is useful for prototyping designs and firmware.

1.1 ADS8568EVM Features

- Contains all support circuitry needed for the ADS8568
- Voltage reference options: internal reference, onboard REF5025, or external reference
- Analog input bipolar voltage supply options: onboard ±14.5 V HV analog supplies or external supply inputs
- Compatible with the TI Modular EVM System

The ADS8568EVM-PDK includes the ADS8568EVM and an Opal Kelly XEM3010-based MMB1 motherboard that can be used with ADCPro™ to quickly evaluate the device.

This manual covers the operation of the ADS8568 device referred to as the *ADS8568EVM* and the *ADS8568EVM-PDK*. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS8568EVM.

1.2 Related Documentation from Texas Instruments

The related documents listed in Table 1 are available for download through the Texas Instruments web site at www.ti.com.

Table 1. Related Documents

Device	Literature Number
ADS8568	SBAS543
OPA2211	SBOS377
TPS65131	SLVS493
REF5025	SBOS410
SN74LVC1G17D	SCES351

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2 QuickStart

This section provides a QuickStart guide to quickly get up and running using ADCPro.

2.1 Default Jumper Settings

A silkscreen detailing the default jumper settings is shown in Figure 2. Table 2 explains the configuration for these jumpers.

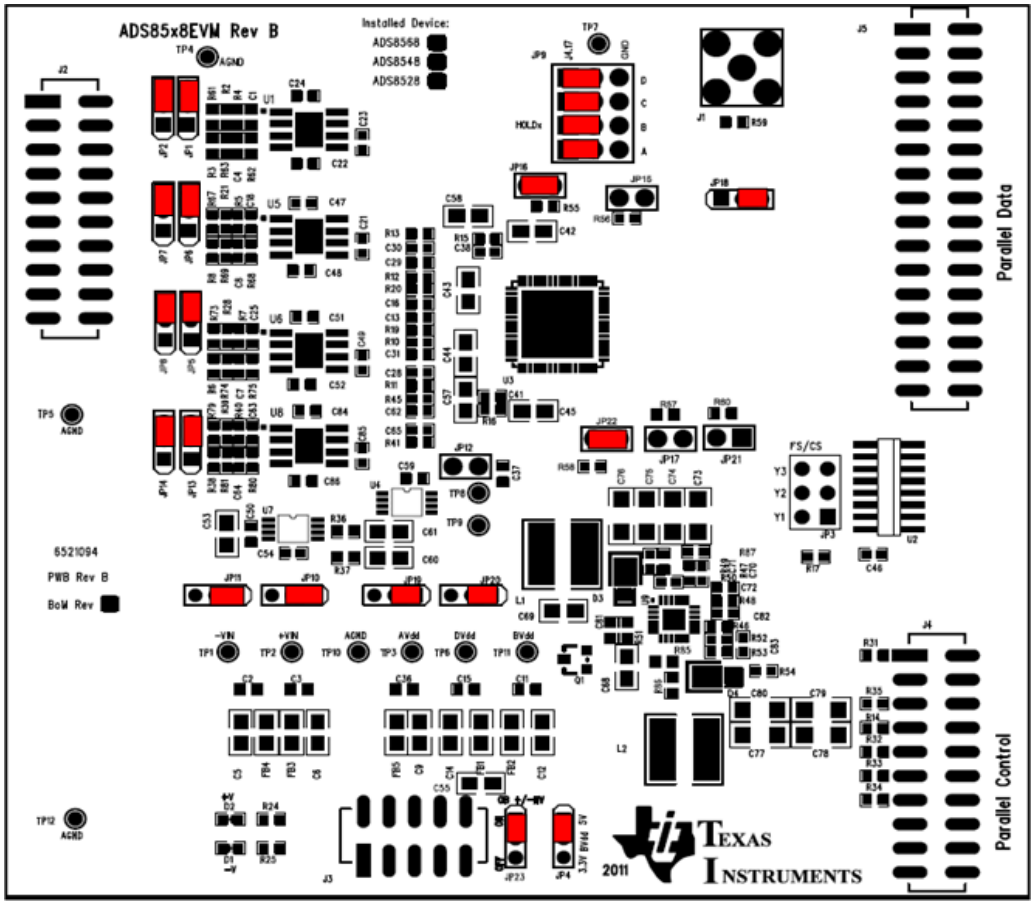

Figure 2. ADS8568EVM Default Jumper Settings

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Table 2. Default Jumper Configuration

Pin Number	Default Position	Switch Description
JP1	Short 2-3	Selects the buffered A0 input configuration
JP2	Short 2-3	Selects the buffered A1 input configuration
JP3	Open	Sets $\overline{CS}$ low with R17
JP4	Short 1-2	Selects +5 VD as the BVDD voltage
JP5	Short 2-3	Selects the buffered C0 input configuration
JP6	Short 2-3	Selects the buffered B0 input configuration
JP7	Short 2-3	Selects the buffered B1 input configuration
JP8	Short 2-3	Selects the buffered C1 input configuration
JP9	Short 1-2, 4-5, 7-8, and 10-11	Conversion start to J4.17 DCTOUT
JP10	Short 1-2	Selects +HVINT for the +VOP AMP supply
JP11	Short 1-2	Selects –HVINT for the –VOP AMP supply
JP12	Open	External reference not connected to REFIO
JP13	Short 2-3	Selects the buffered D0 input configuration
JP14	Short 2-3	Selects the buffered D1 input configuration
JP15	Open	Disables auto-sleep mode
JP16	Closed	Selects hardware mode
JP17	Open	Disables RESET
JP18	Short 2-3	Selects the ±4 VREF range
JP19	Short 1-2	Selects +HVINT for the +HVDD ADC supply
JP20	Short 1-2	Selects –HVINT for the –HVSS ADC supply
JP21	Open	Internal ADC reference enabled
JP22	Closed	Selects parallel interface mode
JP23	Short 1-2	±HVINT (±14 V) onboard supply on

2.2 ADS8568EVM-PDK Kit Operation

To prepare to evaluate the ADS8568 with the ADS8568EVM-PDK, complete the following steps:

1. Verify the jumpers on the ADS8568EVM are as shown in Figure 2 (note that these settings are the factory-configured settings for the EVM).
2. Using the MMB1 Motherboard User's Guide (SLAU372), verify the MMB1 jumpers are in the default position and install the ADCPro and ADS8568EVM plug-in software. Complete hardware connections and driver installation as part of the MMB1 Motherboard User's Guide (SLAU372).
3. Plug the ADS8568EVM into the MMB1. The female portion of J2, J3, J4, and J5 on the EVM align with the respective male connectors J6, J7, J13, and J14 of the MMB1.
4. Connect the included ac adapter to the MMB1.

CAUTION

Do not misalign the pins when plugging the ADS8568EVM into the MMB1. Check the pin alignment of J2, J3, J4, and J5 carefully before applying power to the ADS8568EVM-PDK.

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3 Quick Reference

3.1 Analog Input

Eight of the analog input sources (channels 0 to 7) can be applied directly to header J2 of the ADS8568EVM (top side) or through the analog IO J3 connector on the MMB1 board. Each analog input signal can be configured to connect to the ADS8568 through the OPA2211 inverting, unity-gain buffers (default condition JPx jumpered pins 2 to 3) or directly to the ADS8568 device. Refer to the *Analog Input Circuit* section of the *ADS8568EVM Hardware Details* for more information about the analog input circuit. By default, the device is set up with the 2.5-V internal reference and the ±4x V_{REF} range selected; corresponding to ±10-V range.

3.2 Digital Control

There is a variety of control lines associated with the ADS8568EVM that are user-accessible through various jumpers. The ADS8568 may output the conversion results using a serial or parallel interface. The ADS8568EVM may be set in parallel or serial mode through jumper JP22 and may be configured in hardware or software control mode through jumper JP16.

The operating mode of the device determines which connector pins on connectors J4 and J5 are used to control the converter operation and timing, and which pins on the connector output the digital results.

NOTE: The ADS8568EVM-PDK kit with ADCPro supports the parallel interface mode of operation under hardware mode or software mode control. By factory default, the ADS8568EVM-PDK is configured to operate with the parallel interface (JP22 shunt) under hardware control (JP16 shunt). When using the ADS8568EVM-PDK kit, the parallel interface conversion results are available through connector J5.

3.3 Power Supply

The analog portion of the ADS8568 requires an analog 5-V supply and a bipolar input supply. The 5-V analog voltage supply can be generated by the ac adapter or by applying the +5 VA to the connector of the MMB1 board. The ADS8568EVM is configured at the factory with the onboard ±14.5-V bipolar supply. The user can also select to apply the bipolar supply to the ±VA connectors on the MMB1 board. Please refer to the *Power Supplies* section of the *ADS8568EVM Hardware Details* for more information.

CAUTION

Do not exceed the ±18-VDC bipolar Input supply limit. Damage to the op amps and the ADS8568 can occur if this limit is exceeded.

3.4 Voltage Reference

The ADS8568 has an internal, 2.5-V to 3-V programmable reference. Alternatively, the user can select the onboard 2.5-V reference, REF5025 (U7). The device is set up by default in hardware mode (JP16 closed) with the internal 2.5-V reference enabled (JP21 open). Refer to the *ADS8568 Internal Reference and EVM Onboard Reference* section of the *ADS8568EVM Hardware Details* for more information.

CAUTION

If the REF5025 2.5-V onboard reference is required, the internal reference must be disabled by first shorting JP21 and afterwards installing JP12. Ensure JP12 is open whenever the internal reference is enabled to avoid potential damage to the ADS8568 device.

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4 Using the ADS8568EVM-PDK Plug-In in ADCPro

4.1 Using the ADS8568EVM-PDK Plug-in

The ADS8568EVM-PDK plug-in for ADCPro provides control over all settings of the ADS8568 in parallel interface mode. The ADS8568EVM-PDK plug-in may be used in Hardware mode or Software mode. The user can adjust the ADS8568EVM settings when not acquiring data. During acquisition, all controls are disabled and settings may not be changed. When a setting is changed on the ADS8568EVM plug-in, the setting immediately updates on the board.

Settings on the ADS8568EVM correspond to settings described in the ADS8568 product data sheet.

4.1.1 Operation in Hardware Mode

For proper operation in hardware mode, the user selects *Hardware* mode by clicking on the **Mode** panel. Jumper JP16 must be shunted or closed; refer to Figure 3. The channel range is adjusted in hardware mode by setting jumper JP18: shunt 2-3: ±4x V_{REF} range is selected; shunt 1-2: ±2x V_{REF} range is selected. For proper operation, the user must also ensure that the channel range in ADCPro matches the hardware settings.

When using the internal reference, the user must verify that jumper JP12 is open; JP21 must be open to enable the internal reference. If the onboard REF5025 2.5-V reference is desired, JP21 must be shunted to disable the internal reference and the user must switch to Software mode. The user may input the desired sampling rate on the **Data Rate** panel. The data rate is limited by the ADS8568EVM plug-in software to a maximum of 400 kSPS. The conversion results are available on connector J5.

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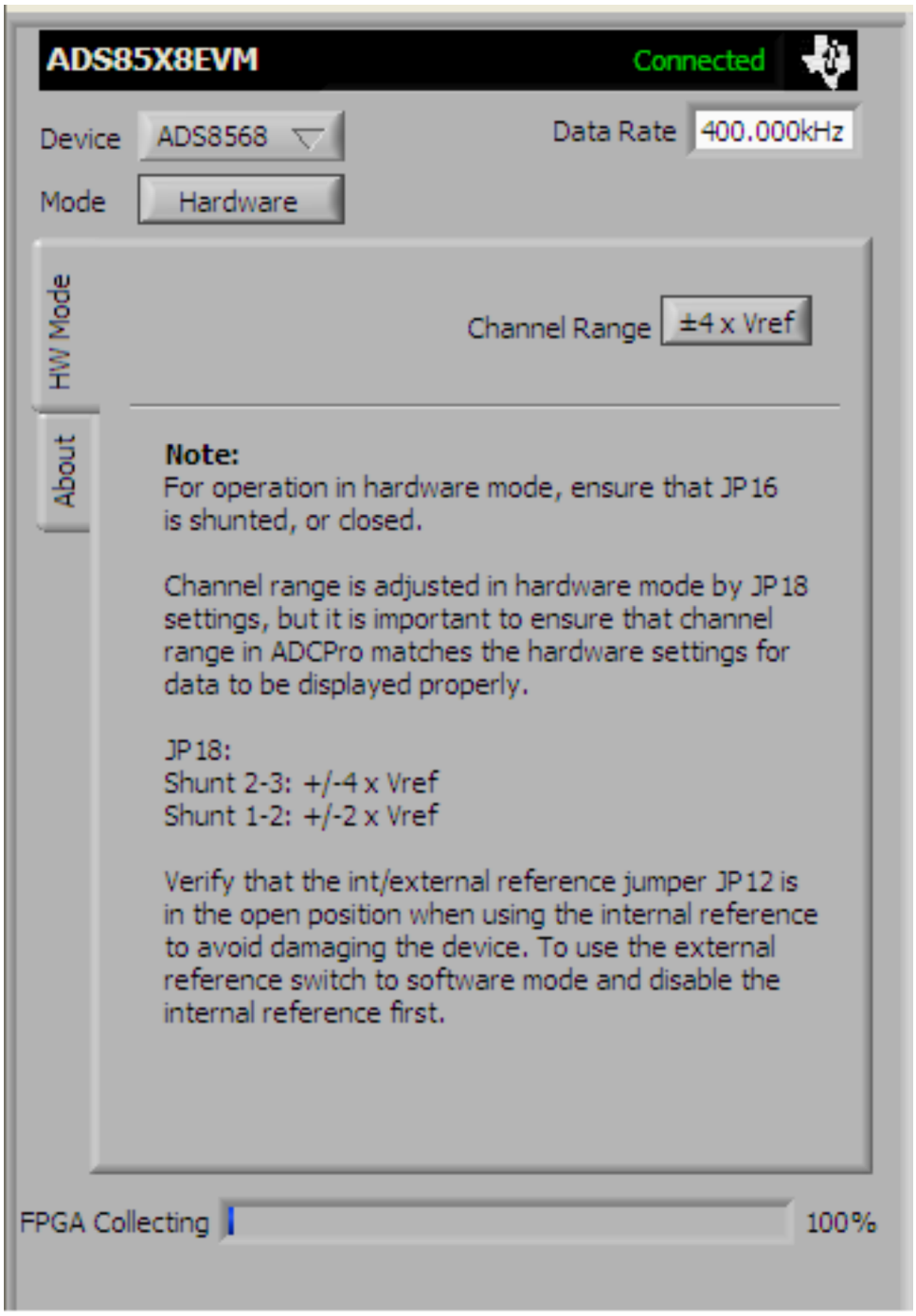
ADS85X8EVM
Connected
Device
ADS8568
Data Rate
400.000kHz
Mode
Hardware
HW Mode
About
Channel Range
±4 x Vref
Note:
For operation in hardware mode, ensure that JP16 is shunted, or closed.
Channel range is adjusted in hardware mode by JP18 settings, but it is important to ensure that channel range in ADCPro matches the hardware settings for data to be displayed properly.
JP18:
Shunt 2-3: +/-4 x Vref
Shunt 1-2: +/-2 x Vref
Verify that the int/external reference jumper JP12 is in the open position when using the internal reference to avoid damaging the device. To use the external reference switch to software mode and disable the internal reference first.
FPGA Collecting
100%

Figure 3. Operation in Hardware Mode

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4.1.2 Operation in Software Mode

For proper operation in software mode, the user selects *Software* mode by clicking on the **Mode** panel. Jumper JP16 must be open, as shown in Figure 4.

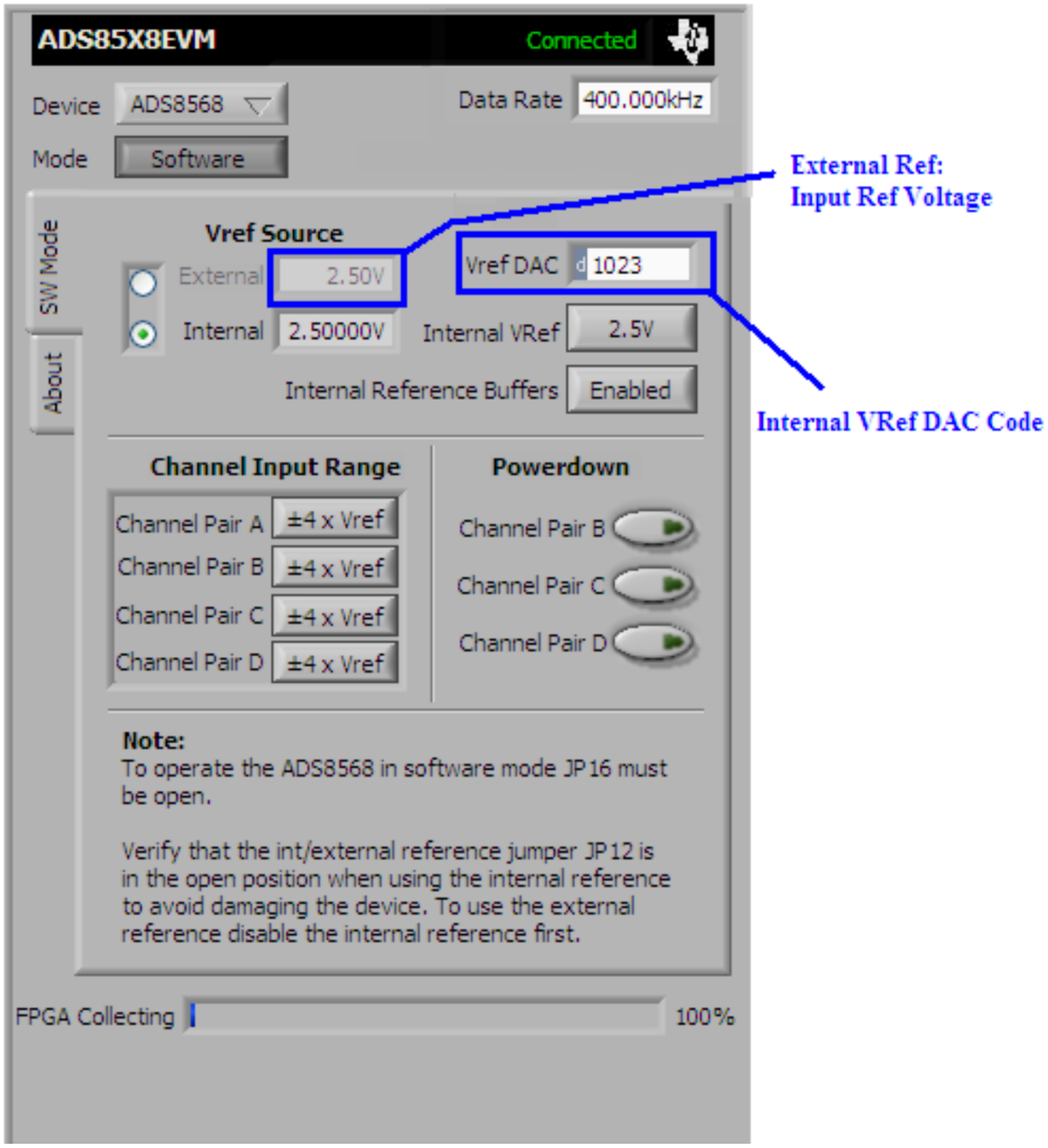

Figure 4. Operation in Software Mode

When using the internal reference, the user must verify that jumper JP12 is open and select *Internal* in the *Vref Source* control. The *Internal Reference Buffers* must be enabled by selecting the appropriate panel. The user may choose either the 2.5 V or 3.0 V internal V_{REF}. In addition, the user may program the V_{REF} DAC to adjust the voltage reference by placing the code value (as determined by Equation 1) in the **Vref DAC** panel provided.

$$V_{REF} = \text{Range} \times (\text{Code} + 1)/1024 \quad (1)$$

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Code is the decimal value of the DAC register content. To ensure proper performance, the DAC output voltage should not be programmed below 0.5 V.

If the external reference is desired, the user must disable the internal reference first by selecting *External*. The user may either install jumper J12 to connect the onboard 2.5-V REF5025 reference or connect an external reference. The allowed external reference range is from 0.5 V to 3.025 V. The user must input the reference voltage in the External **Vref Source** panel provided in the screen in order for ADCPro to display the conversion results properly.

When the device is operating in software mode, the channel range is adjusted for each channel pair by selecting either ±4x V_{REF} or ±2x V_{REF} in the **Channel Input Range** panel. Each device channel pair (except channel pair A, which is the master channel pair and is always active) can be individually switched off using the **Powerdown** panel provided. The user may input the desired sampling rate on the **Data Rate** panel. The data rate is limited by the ADS8568EVM plug-in software to a maximum of 400 kSPS. The conversion results are available on connector J5.

5 ADS8568EVM Hardware Details

The ADS8568EVM is designed to easily interface with multiple control platforms. Dual-row, header/socket combinations at J2, J3, J4, and J5 allow connection to external circuitry for evaluation and debug.

5.1 Analog Input Circuit

The circuit at the analog input of the ADS8568EVM board consists of four independent OPA2211 dual operational amplifiers. The OPA2211 dual op amps may be powered from an onboard ±14.5-V analog supply or from an external supply. The amplifiers are configured as inverting, unity-gain buffers by default. The OPA2211 buffer input circuit is shown in Figure 5. This circuit is used in all eight input channels. Jumper JPx can be used to bypass the input buffer circuit.

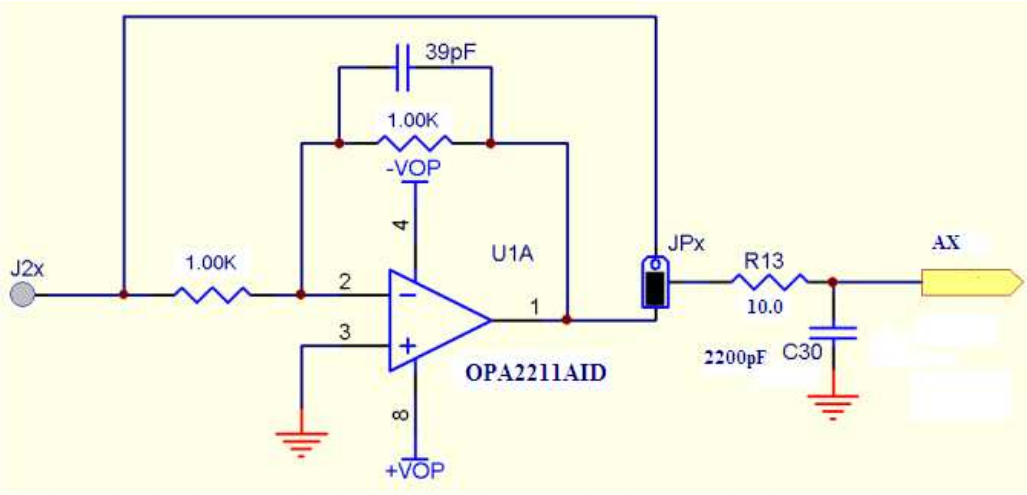

Figure 5. Analog Input Schematic

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5.2 ADS8568 Internal Reference and EVM Onboard Reference

The ADS8568 has an internal, programmable 2.5-V or 3-V internal reference. Alternatively, the user can select the onboard 2.5-V reference, REF5025 (U7).

- When the device is set up in hardware mode (JP16 closed), the internal fixed 2.5-V reference is enabled through the REFEN pin (JP21 open). Refer to Figure 6 for the jumper location. The channel range is adjusted in hardware mode by the JP18 settings:
  - JP18 shunt 2-3: ±4x V_{REF} range selected
  - JP18 shunt 1-2: ±2x V_{REF} range selected

NOTE: The device is configured at the factory in hardware mode with a 2.5-V reference and a ±4x V_{REF} range. The **Operation in Hardware Mode** section provides more detailed information about the hardware mode of operation.

- When the device is set up in software mode (JP16 open), the user can select either the internal 2.5-V or 3.0-V programmable reference and choose either the ±4x V_{REF} or ±2x V_{REF} range through the software panel on the ADS8568EVM Plug-In.
- If the onboard REF5025 2.5-V reference is desired, the internal reference must first be disabled (in hardware mode, J21 must be shunted to disable the reference). The ADS8568EVM provides an onboard 2.5-V reference via U7. To use the REF5025 reference, a shunt jumper must be placed on JP12. Test points TP8 and TP9 are provided to allow the user to monitor the reference voltage (either internal or the REF5025) and may also be used to connect a user-provided reference voltage in the range of 0.5 V to 3.025 V.

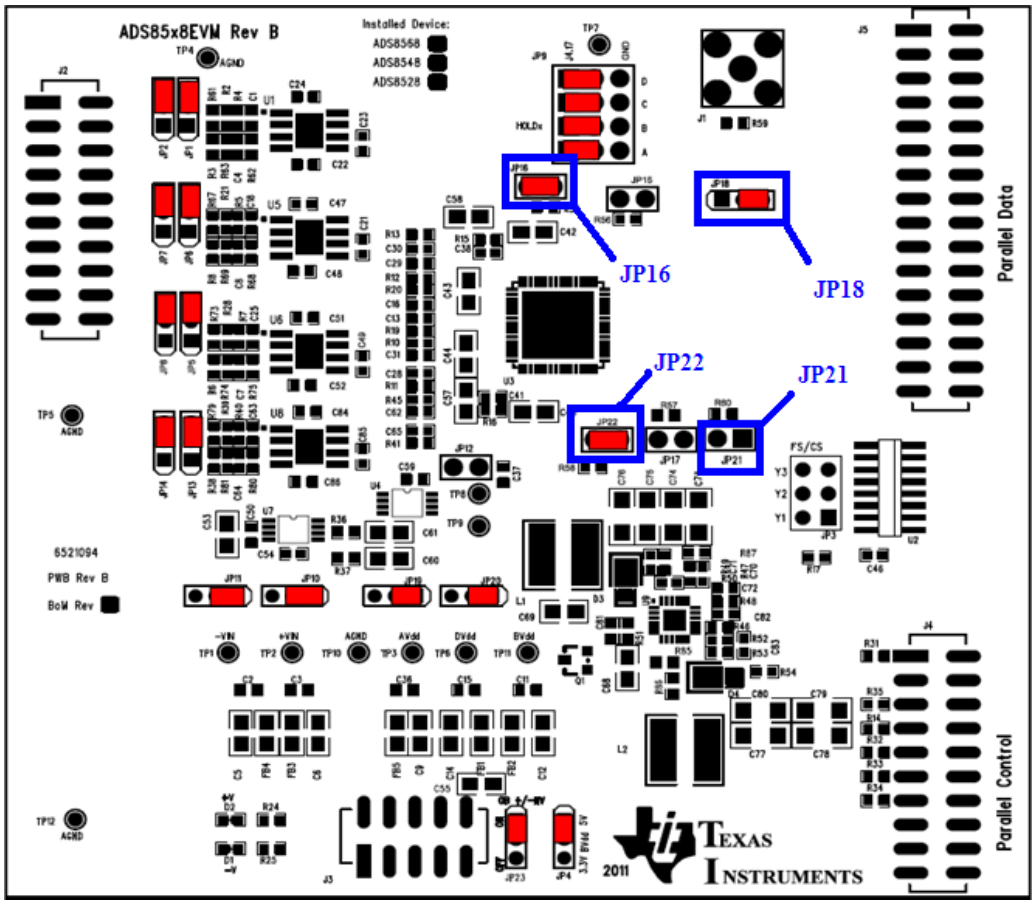

Figure 6. Jumpers JP16, JP18, JP21, and JP22

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5.3 Power Supplies

The ADS8568EVM-PDK is configured at the factory with an on-board bipolar analog input ±14.5 V switching supply (±HV), a +5-V AV_{DD} analog supply, and either a +5 BV_{DD} or +3.3 V_{DD} supply. For ADS8568EVM stand-alone operation, power sources can be applied through connector J3 on the board. Table 3 shows the various supply connections on connector J3.

Table 3. Connector J3: Power-Supply Inputs

Signal	Pin Number		Signal
+VA Connects to HVDD	1	2	(+VA) Connects to HVSS
(+5 VA) Connects to AV_{DD}	3	4	Unused
DGND	5	6	AGND
Unused	7	8	Unused
+3.3 V optional BV_{DD}	9	10	+5 V optional BV_{DD}

5.3.1 Bipolar Analog Input Supplies

The board is configured from the factory with a ±14.5-V switching supply to generate the HV analog bipolar input ±14.5-V supply. The onboard ±14.5 V is generated via the TPS65131 positive and negative dc to dc converter. The user could also provide power to the HV supplies and onboard buffers from a well-regulated, external linear supply that has current-limiting capabilities.

The HVDD and HVSS supplies to the ADS8568 can be selected through jumpers JP19 and JP20. The supplies to the OPA2211 buffers can be selected through jumpers JP10 and JP11. If the user desires to use the external linear supply; the switching power supply may be disabled by placing jumper JP23 to the *OFF* position. Ensure all power is off before manipulating the power-supply jumpers. Table 4 describes the bipolar input supply jumpers.

Table 4. Analog Bipolar Input Supply Jumpers

Pin Number	Default Position	Switch Description
JP10	Short 1-2	1-2 On-board +HVINT to OPA2211 buffers 2-3 External +HV supply to OPA2211buffers
JP11	Short 1-2	1-2 On-board -HVINT to OPA2211 buffers 2-3 External -HV supply to OPA2211buffers
JP19	Short 1-2	1-2 On-board +HVINT to HVDD supply on ADS8568 2-3 External +HV to HVDD supply on ADS8568
JP20	Short 1-2	1-2 On-board +HVINT to HVDD supply on ADS8568 2-3 External +HV to HVDD supply on ADS8568

CAUTION

Do not exceed the ±18-VDC bipolar input supply limit. Damage to the op amps and the ADS8568 can occur if this limit is exceeded.

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5.3.2 Analog +5-V Supply

The ADS8568EVM board requires an independent +5-V supply to power the analog portion of the DUT, the external reference, and the external reference buffer. This voltage is applied through J3 (pin 3) and is denoted as AVDD. This supply can be monitored at test point TP3.

5.3.3 Digital Power: Buffer I/O Supply

The buffer I/O supply of the ADS8568EVM-PDK is provided through connector J3. Connector J3 has a +3.3-V and +5-V digital supply defined on pins 9 and 10, respectively. Jumper JP4 on the EVM allows the user to select the default +5.5 V or 3.3 V for the device BV_{DD} source. This voltage is also applied to the remaining digital circuitry on the EVM. Figure 7 shows jumper JP4 configured for the 3.3-VD buffer I/O supply.

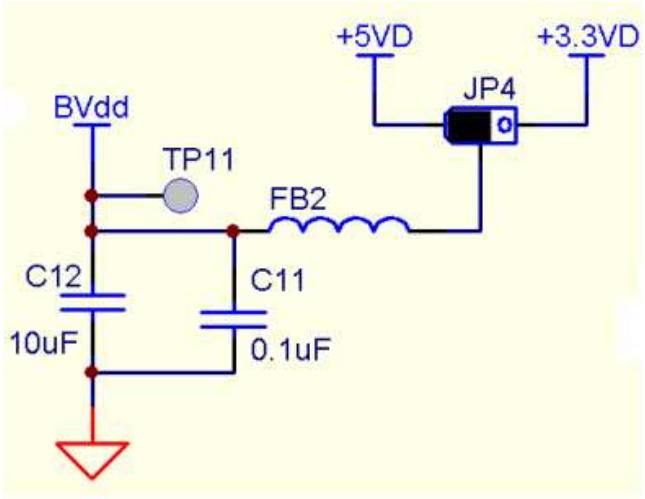

Figure 7. BV_{DD} Voltage Selection

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5.4 Digital Controls: J4 and J5

The digital inputs and outputs of the EVM are provided through connectors J4 and J5. The ADS8568EVM-PDK plug-in supports the parallel interface of operation.

5.4.1 Parallel Control: Connector J4

Connector J4 contains parallel control signals such as write enable and read enable. Four address lines are also provided to allow the stacking of multiple ADS8568EVMs. The signals applied to this connector are routed through U7 when the device is set up in the parallel interface mode of operation (JP22 closed). Table 5 describes the control lines found on J4.

Table 5. Connector J4: Parallel Control

Pin Number	Signal	Description
J4.1	DC_CNTL	G2A input to address decoder U3; default low by pull-down resistor R_{33}.
J4.3	DC_AWE	Active low write enable input to ADS8568; used with $\overline{CS}$ to write to the configuration register.
J4.5	DC_ARE	Active low read enable input to ADS8568; used with $\overline{CS}$ to read from the parallel data bus.
J4.7	DC_A0	3-line to 8-line address decoder input A.
J4.9	DC_A2	3-line to 8-line address decoder input B.
J4.11	DC_A3	3-line to 8-line address decoder input C.
J4.13	N/C	3-line to 8-line address decoder input G1; must be high to enable address line decoder.
J4.15	DC_A3	No connection
J4.17	DC_TOUT	CONVST_A/B/C/D inputs when shunt jumpers are placed in the respective default states on JP9, as described in Table 2.
J4.19	DC_INTa	Interrupt source to host processor; connects directly to pin 18 (BUSY) of the ADS8568.
J4.2 through J4.20 (even)	DGND	These pins are connected to digital ground.

5.4.2 Parallel Data: Connector J5

Connector J5 contains parallel interface output data lines. Table 6 lists the parallel data output found in connector J5.

Table 6. Connector J5: Parallel Interface Data Ouput

Pin Number	Signal	Description
J5.1 through J5.31 (odd)	DCD[15:0]	16-bit parallel data bus used when writing to or reading from the ADS8568 in parallel mode.
J4.3	DGND	These pins are connected to digital ground.

6 Bill of Materials, Layout, and Schematic

6.1 Bill of Materials

Table 7 lists the ADS8568EVM bill of materials.

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Table 7. Bill of Materials

Item	Quantity	Designator	Description	Manufacturer	Part Number
1	1	N/A	Printed wiring board	TI	6521094
2	8	C1, C18, C19, C25-C27, C63, C66	Capacitor, ceramic, 39 pF, 50 V, 5%, C0G, 0603	Murata	GRM1885C1H390JA01D
3	25	C2, C3, C11, C15, C22, C24, C32-C36, C38-C41, C46-C48, C50-C52, C59, C81, C84, C86	Capacitor, ceramic, 0.1 µF, X7R, 50 V, 10%, 0603	Murata	GRM188R71H104KA93D
4	0	C4, C7, C8, C10, C17, C20, C64, C67	Not installed	—	—
5	13	C5, C6, C9, C12, C14, C42-C45, C53, C57, C58, C61	Capacitor, ceramic, 10 µF, X5R, 16 V, 20%, 0805	TDK	C2012X5R1C106M
6	8	C13, C16, C28-C31, C62, C65	Capacitor, ceramic, 2200 pF, 50 V, 5%, C0G, 0603	Murata	GRM1885C1H222JA01D
7	5	C21, C23, C49, C54, C85	Capacitor, ceramic, 1 µF, X5R, 35 V, 10%, 0603	Taiyo Yuden	GMK107BJ105KA-T
8	1	C37	Capacitor, ceramic, 0.47 µF, X5R, 10 V, 10%, 0603	Murata	GRM188R61A474KA61D
9	2	C55, C60	Capacitor, ceramic, 22 µF, X5R, 6.3 V, 10%, 0805	Taiyo Yuden	JMK212BJ226KG-T
10	1	C68, C69	Capacitor, ceramic, 4.7 µF, 25 V, X5R, 0805	Murata	GRM21BR61E475KA12L
11	2	C70, C72	Capacitor, ceramic, 0.01 µF, X7R, 50 V, 10%, 0603	Murata	GRM188R71H103KA01D
12	2	C71, C83	Capacitor, ceramic, 150 pF, 50 V, C0G, 0603	TDK	C1608C0G1H151J
13	8	C73-C80	Capacitor, ceramic, 4.7 µF, 25 V, X7R, 10%, 1206	TDK	C3216X7R1E475K
14	1	C82	Capacitor, ceramic, 0.22 µF, 16 V, X7R, 10%, 0603	TDK	C1608X7R1C224K
15	2	D1, D2	LED, 565nm, green diff, 0603, SMD	Lumex	SML-LX0603GW-TR
16	2	D3, D4	MBRM120, Schottky, 1 A, 20 V, PowerMite	On Semi	MBRM120ET3G
17	5	FB1-FB5	Ferrite chip, 600 Ω, 500 mA, 0805	TDK	MMZ2012R601A
18	1	J1	Connector, SMA, jack, straight PCB	Amphenol	132134
19	1	J1	Connector, SMA, jack, straight PCB	Emerson	142-0701-201
20	2	J2, J4 (Top)	10-pin, dual row, SM header (20 posible)	Samtec	TSM-110-01-T-DV-P
21	2	J2, J4 (Bottom)	10-pin, dual row, SM header (20 posible)	Samtec	SSW-110-22-F-D-VS-K
22	1	J3 (Top)	5-pin, dual row, SM header (10 posible)	Samtec	TSM-105-01-T-DV-P
23	1	J3 (Bottom)	5-pin, dual row, SM header (10 posible)	Samtec	SSW-105-22-F-D-VS-K
24	1	J5 (Top)	16-pin, dual row, SM header (32 posible)	Samtec	TSM-116-01-T-DV-P
25	1	J5 (Bottom)	16-pin, dual row, SM header (32 posible)	Samtec	SSW-116-22-F-D-VS-K
26	15	JP1, JP2, JP4-JP8, JP10, JP11, JP13, JP14, JP18-JP20, JP23	3-pin, 2-mm header	Samtec	TMM-103-01-T-S
27	1	JP3	3-pin, dual row, header (6 posible)	Samtec	TSW-103-07-T-D
28	1	JP9	4-pin, triple row, header (12 posible)	Samtec	TSW-104-07-T-T
29	6	JP12, JP15-JP17, JP21, JP22	2-pin, 0.1-inch header	Samtec	TSW-102-07-T-S

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Table 7. Bill of Materials (continued)

Item	Quantity	Designator	Description	Manufacturer	Part Number
30	2	L1, L2	Power inductors, 5.3 µH, 1.90 A	Sumida	CDRH5D28NP-5R3NC
31	1	Q1	MOSFET, P-channel, 20 V, 3.7 A, SOT23-3	Vishay/Siliconix	SI2323DS-T1-E3
32	24	R1, R4, R5, R7, R14, R17, R18, R27, R31-R35, R40, R44, R60, R61, R64, R67, R70, R73, R76, R79, R82	Resistor, 1 kΩ, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-071KL
33	10	R10-R13, R15, R16, R19, R20, R41, R45	Resistor, 10 Ω, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-0710RL
34	0	R2, R3, R6, R8, R9, R21-R23, R26, R28-R30, R38, R39, R42, R43, R85	Not installed	—	—
35	5	R36, R55-R58	Resistor, 10 kΩ, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-0710KL
36	2	R24, R25	Resistor, 2 kΩ, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-072KL
37	1	R37	Resistor, 1 Ω, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-071RL
38	1	R46	Resistor, 130 kΩ, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-07130KL
39	20	R47, R48, R54, R62, R63, R65, R66, R68, R69, R71, R72, R74, R75, R77, R78, R80, R81, R83, R84, R86	Resistor, 0 Ω, 1/10 W, 0603, SMD	Yageo	RC0603JR-070RL
40	1	R49	Resistor, 1 MΩ, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-071ML
41	1	R50	Resistor, 90.9 kΩ, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-0790K9L
42	1	R51	Resistor, 100 Ω, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-07100RL
43	1	R52	Resistor, 1.50 MΩ, 1/10 W, 1%, 0603	Yageo	RC0603FR-071M5L
44	2	R53, R87	Resistor, 51.1 kΩ, 1/10 W, 1%, 0603, SMD	Yageo	RC0603FR-0751K1L
45	1	R59	49.9 Ω, 1/10 W, 1% 0603, SMD	Yageo	RC0603FR-0749R9L
46	6	TP1-TP3, TP6, TP8, TP11	Test point, PC, mini, 0.040"D, red	Keystone	5000
47	6	TP4, TP5, TP7, TP9, TP10, TP12	Test point, PC, mini, 0.040"D, black	Keystone	5001
48	4	U1, U5, U6, U8	IC, op amp, precision, DL, LNLP, 8-SOIC	TI	OPA2211AIDDA
49	1	U2	IC, 3-8 line, decodr/demux, 16-SOIC	TI	SN74AHC138D
50	1	U3	ADS8568, ADS85x8, *16/14/12-Bit, 8-Channel, Simultaneous Sampling Bipolar Input ADC*	TI	ADS8568SRGE
51	1	U4	IC, op amp, GP, R-R, 38 MHz, SGL, 8-MSOP	TI	OPA350EA/250
52	1	U7	IC, precision, VREF, 2.5 V, LN/LD, MSOP	TI	REF5025AIDGKT
53	1	U9	IC, converting, DC/DC, pos/neg, 24-QFN	TI	TPS65131RGER
54	6	N/A	0.100, shunt—black shunts	3M	969102-0000-DA
55	13	N/A	2-mm shunt	Samtec	2SN-BK-G

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6.2 Layout

Figure 8 through Figure 12 show the PCB layout of the ADS8568EVM (not to scale).

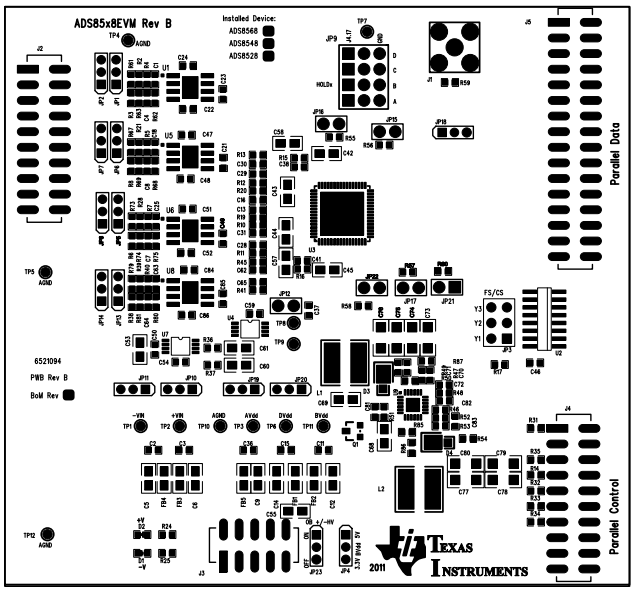

Figure 8. ADS8568EVM: Silkscreen (Top Layer)

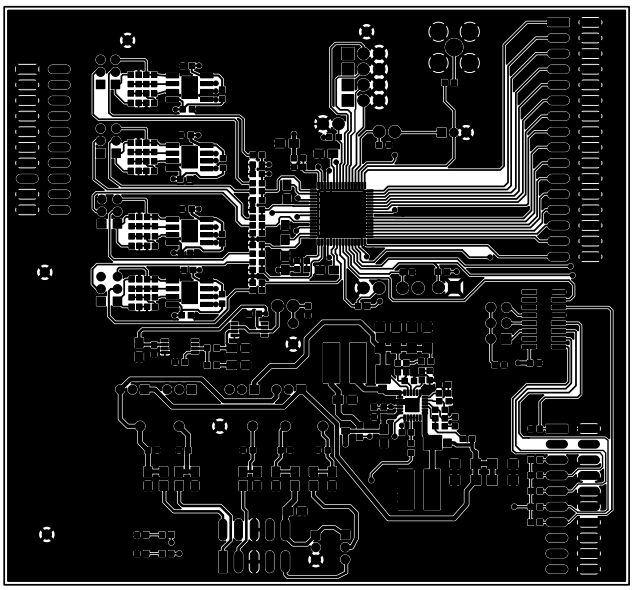

Figure 9. ADS8568EVM: Top

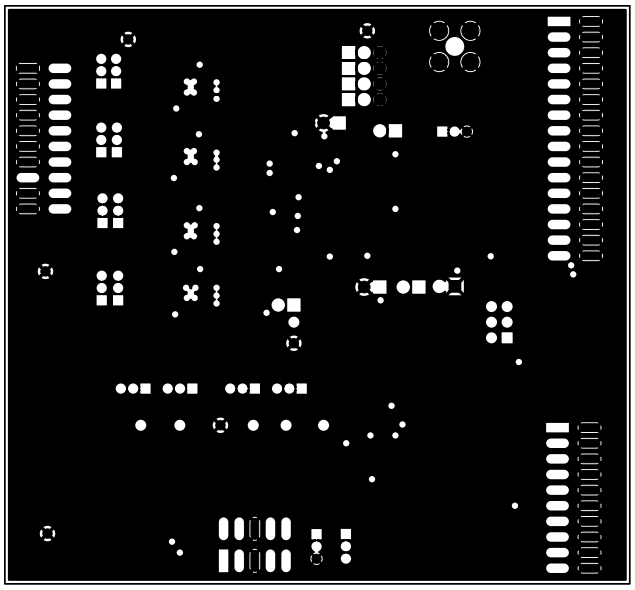

Figure 10. ADS8568EVM: Internal GND Layer 1

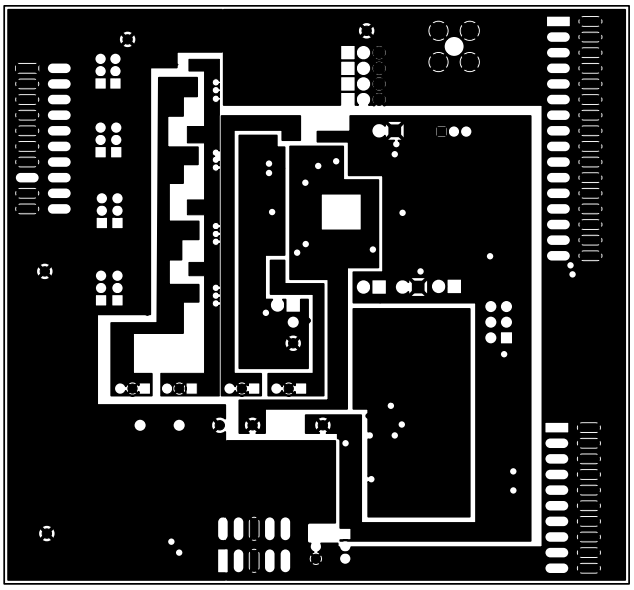

Figure 11. ADS8568EVM: Internal Layer 2

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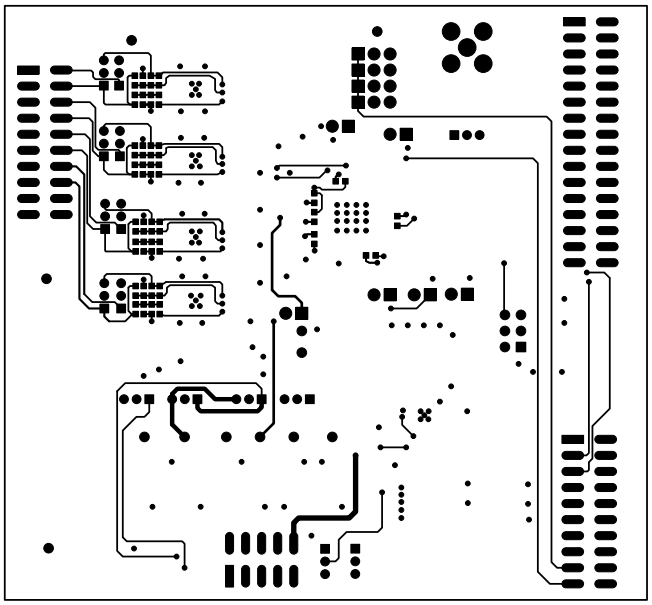

Figure 12. ADS8568EVM: Silkscreen (Bottom Layer)

6.3 Schematic

Figure 13 and Figure 14 show complete schematics for the ADS8568EVM.

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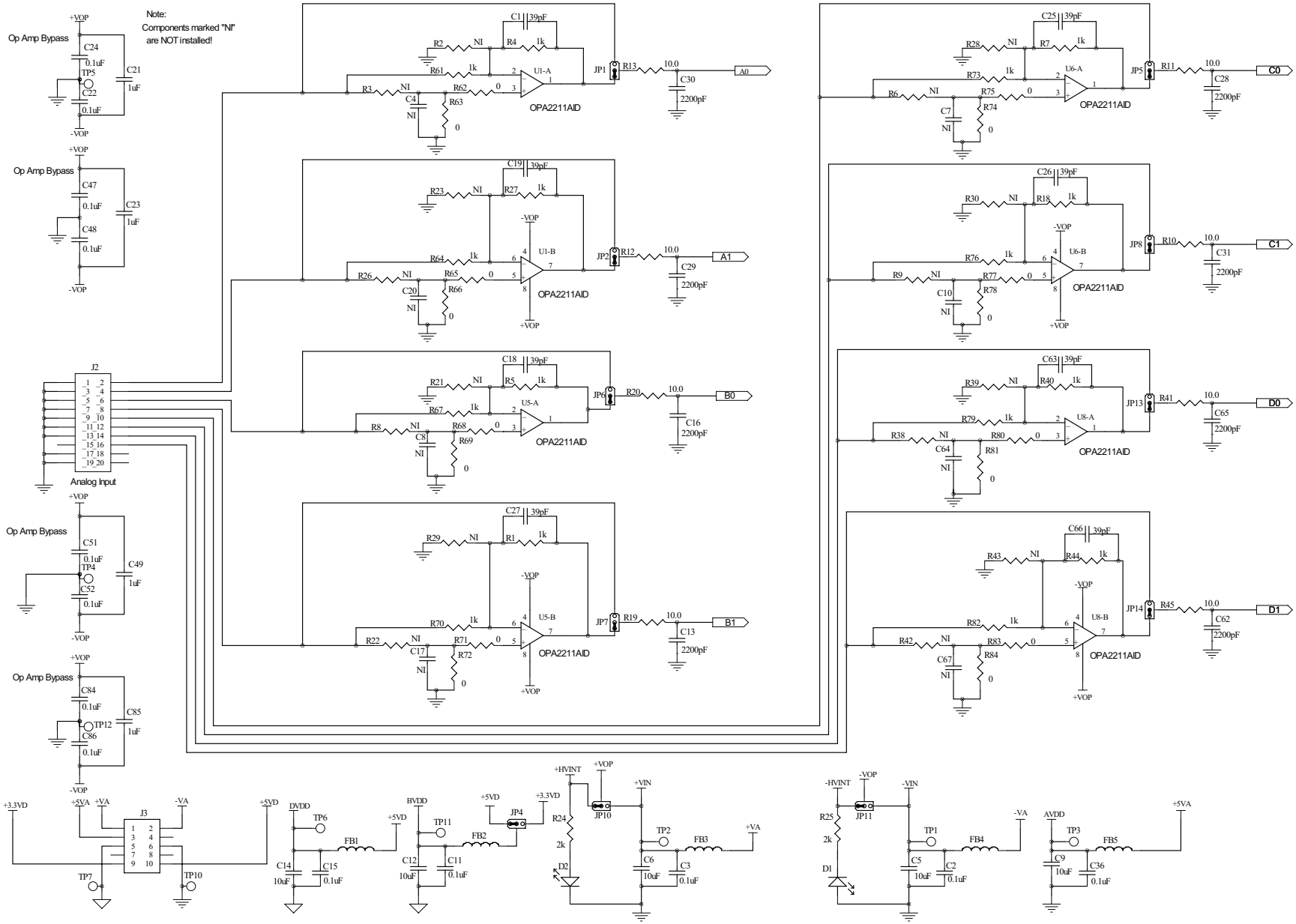

Figure 13. ADS85x8EVM: Schematic 1

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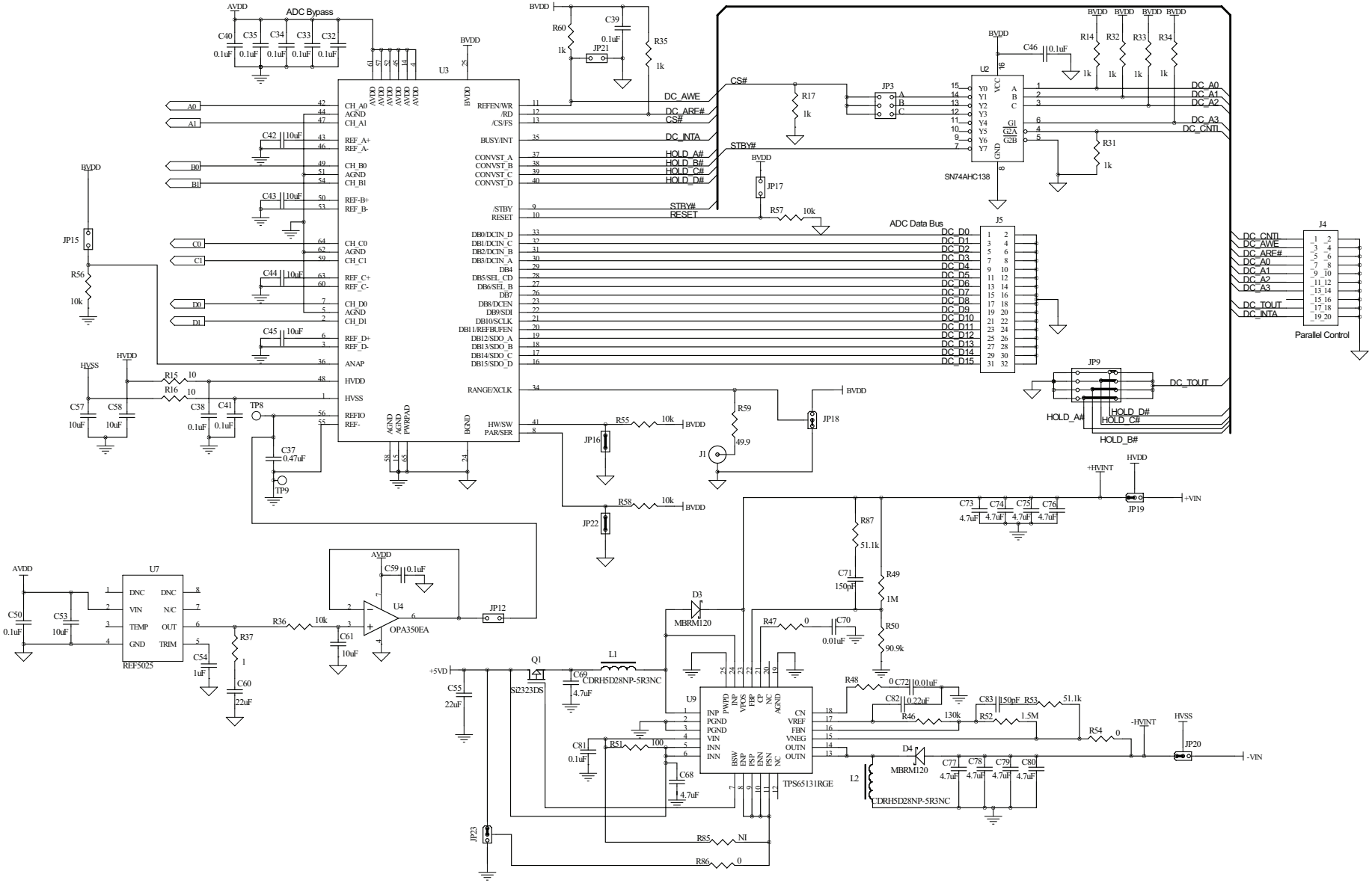

Figure 14. ADS85x8EVM: Schematic 2

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Revision History

Changes from Original (July 2011) to A Revision	Page
• Changed document title to ADS8568EVM-PDK	1
• Changed entire document	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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